IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region;

a first impurity doped layer of a first conductivity type ~~formed in said channel region~~, the channel region being formed in said first impurity doped layer of the first conductivity type between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said three impurity doped layers make up a multilayer lamination structure with two p-n junctions, one between said first and said second impurity doped layers and the other between said second and said third impurity doped layer, wherein

said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, and wherein

said second impurity doped layer is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers.

2. (Original) The device according to claim 1, wherein said first impurity doped layer is set in impurity concentration and thickness to be fully depleted upon formation of a channel inversion layer.

3. (Original) The device according to claim 1, wherein said first impurity doped layer is set in impurity concentration and thickness to be partially depleted upon formation of a channel inversion layer.

4. (Original) The device according to claim 1, wherein each of said first and second impurity doped layers is formed by ion implantation of an impurity into an undoped semiconductor layer as has been epitaxially grown on said semiconductor substrate with said third impurity doped layer formed therein.

5. (Original) The device according to claim 1, wherein said second impurity doped layer is selectively formed in a region immediately beneath said gate electrode.

6. (Original) The device according to claim 4, wherein

said second impurity doped layer is selectively formed in a region of said undoped semiconductor layer just beneath said gate electrode, and wherein

said source/drain diffusion layers are formed so that a bottom surface of the low resistivity region resides within said undoped semiconductor layer whereas a bottom surface of the extension region is in contact with said second impurity doped layer.

7. (Original) The device according to claim 1, further comprising:

fourth impurity doped layers of the first conductivity type as embedded to be in contact with the extension regions of said source and drain diffusion layers.

8. (Original) The device according to claim 1, wherein the low resistivity regions of said source/drain diffusion layers are formed to have top surfaces higher in level than said gate dielectric film.

9. (Original) The device according to claim 1, wherein said gate electrode has a metal film as contacted with the gate dielectric film.

10. (Original) The device according to claim 2, wherein said gate electrode is formed of a metal film.

11. (Original) The device according to claim 3, wherein said gate electrode is formed of a poly-silicon film.

12. - 46. (Cancelled).

47. (New) A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region;

a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer;

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer; and

a fourth impurity doped layers of the first conductivity type as embedded to be in contact with the extension regions of said source and drain diffusion layers, wherein

said three impurity doped layers make up a multilayer lamination structure with two p-n junctions, one between said first and said second impurity doped layers and the other between said second and said third impurity doped layer, wherein

said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, and wherein

said second impurity doped layer is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers.

48. (New) A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region;

a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer, and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said three impurity doped layers make up a multilayer lamination structure with two p-n junctions, one between said first and said second impurity doped layers and the other between said second and said third impurity doped layer, wherein

said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, wherein

said second impurity doped layer is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers, and wherein

the low resistivity regions of said source/drain diffusion layers are formed to have top surfaces higher in level than said gate dielectric film.